12.2 A Capacitive Hybrid Flip-Chip ASIC and Sensor for Fingerprint, Navigation and Pointer Detection

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A number of CMOS sensor chips for fingerprint identification have been designed. They are matrix 2D sensors that require a large silicon area (30mm² to 225mm²), making it difficult to embed these chips in small devices [1] [2].

A hybrid module, consisting of a silicon sensor substrate, flip-chipped to a high density, small size, mixed signal CMOS ASIC, is presented. The architecture integrates three functions: fingerprint, navigation and pointer detection.

The module combines linear scanner ac-capacitive fingerprint sensor technology [3] with ASIC and flip-chip technology to provide scan-type fingerprint access control and pointer for on-screen point-and-click navigation features. The approach uses an optimized solution for these technologies, resulting in a cost-effective module.

The sensor consists of a linear structure of metal plates covered with a thin mechanically strong dielectric layer. Unlike previous designs, the sensor is implemented as a linear scanner and the ASIC processes only 256 channels. This approach reduces considerably the silicon area. The finger is stimulated by an ac signal via the stimulation electrode, and each sensor plate measures the modulated signal, proportional to the variable capacitance C_{FS} due to the pattern of ridges and valleys. The capacitance is measured as the change in voltage that results when a fixed carrier frequency is modulated by the capacitance variations of the fingerprint pattern. As a user pulls a finger over the module, the sensors in the row measure the capacitance of each contact point of the finger surface with the sensor. Additional sensors are used to detect the speed of the finger movement. From this, only sampled line with a distance of 50μm to the previous line is inserted into the reconstructed image, creating equal scaling in both axes. Figure 12.2.1 shows a cross section of the module. The fingerprint/navigation/pointer ASIC architecture is shown in Fig. 12.2.2.

The analog module is implemented as a set of channels each corresponding to one pixel of the sensor. The input signal is generated when the finger establishes a connection between the stimulation electrode and the sensor. The ac signal is a sinus (65kHz-160kHz), generated internally. Each channel consists of a low noise amplifier (LNA), a multiplexer and a phase sensitive amplifier (PSA).

The LNA has high input impedance to match the impedance of the finger and reads the low-level electrical signals. The LNA operates at 2.5V with an open loop gain of 80dB. A global bias circuit provides the bias currents.

The ASIC design is based on a patent-pending concept of pyramidal multiplexing channels into a common analog bus with N lines that are fed to an analog-to-digital converter (ADC) via a second multiplexer [4]. The first group of multiplexers switches input channels synchronously to the start of a cycle period of the sinus generator. The second multiplexer selects one envelope at a time and forwards it to the ADC, which converts N envelopes to a digital representation within one cycle period. The detection of the envelope of the signal representing the finger impedance is achieved by the PSAs. By using a sampler type PSA, a low-pass filter (LPF) is not required. The PSA is controlled by a strobe signal (PSACL), digitally generated. The PSACL phase is controlled in order to compensate the phase shifts, so the signal representing the finger impedance is sampled on the maximum amplitude.

The ASIC incorporates an activation cell that provides an Activation signal used by the host device as an interrupt indicating the point in time when a finger is detected on the sensor surface. The cell assures power control for operating the active circuit blocks. In the initial state the sensor is in sleep mode, characterized by low power consumption with the activation cell waiting.

Figure 12.2.3 shows a block diagram of the digital part. The Analog Front Control module controls the top-level behavior of the ASIC. The Time module generates all timing signals to the analog module and controls the timing for the digital data processing. The module generates the sinus values to the DAC for calibration and stimulation. The RAM receives ADC samples from the analog module (buffered in the Time module) and processes these samples. The LVDS module serializes data from RAM into SPI or LVDS serial format and processes data for use in these formats. The Clock module generates the clocks and associated signals for all the logic except the I2C module. The I2C module is used as a control interface for the ASIC.

The ASIC has a calibration unit for sensor initialization that suppresses the influence of process on ASIC and sensor surface. Using the calibration, the sensing circuit corrects process/parameter variations and offset/gain variance due to the sensor position.

The system accepts a large range of individual fingerprints and various finger conditions including deviations of finger due to movements over the sensor. Software algorithms take these elements into account to achieve high identification accuracy and image enhancement.

The software functions for finger recognition, pointer and navigation are compatible with the processing power of digital baseband processors used in mobile terminal design.

The sensor substrate and the image/navigation/pointer sensors on the topside of the module are shown in Fig. 12.2.4. The backside micrograph of the module with the flip-chipped ASIC/sensor is shown in Fig. 12.2.5.

The ASIC was implemented using a 0.25mm 2P 5M CMOS. The small size, compared with other implementations (147μm²), [1] allows the addition of an embedded processor on chip, while keeping the module cost low. Performance is summarized in Fig. 12.2.6 and a fingerprint image captured by the device is shown in Fig. 12.2.7.

Acknowledgements
The authors acknowledge the contribution of ST Microelectronics, IDEX and SINTEF for their commitment in implementing an idea and concentrating research and development efforts into a commercial viable product.

References
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[3] Fingerprint Sensor, International Patent Application no. PCT/NO98/00182 Filing date: 12 June 1998
[4] Multicycle Multiplexing and Demodulation, European Patent Application: N°02291025.1 Filing date: 23 April 2002

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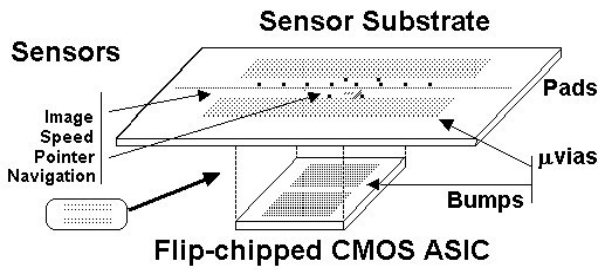

Figure 12.2.1: Cross section of the module.

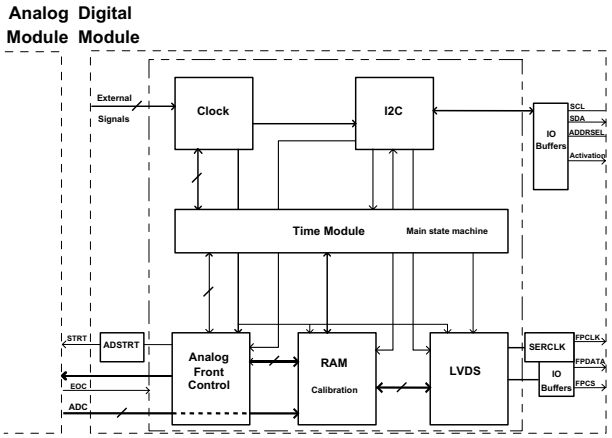

Figure 12.2.3: Digital core architecture.

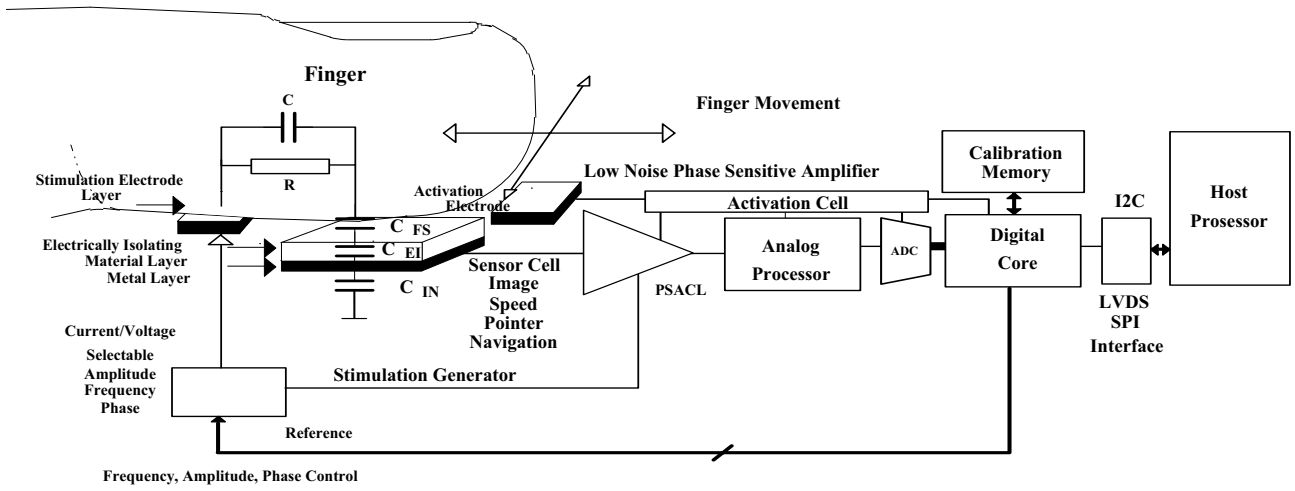

Figure 12.2.2: Module architecture.

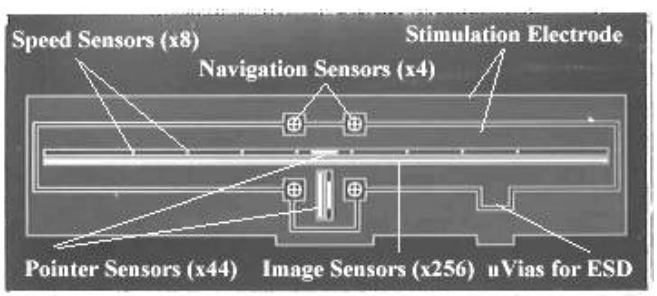

Figure 12.2.4: Module topside micrograph.

Figure 12.2.5: Module backside micrograph.

Sensor size: 15x7mm^2

ASIC size: 18 mm^2

Image resolution: 500dpi

Operating voltage: analog 2.5V, digital 1.5V

ESD resistance: >15kV

Operating temperature range: -20 to 70 °C

Consumption: 30mA peak

Figure 12.2.6: Module performance.

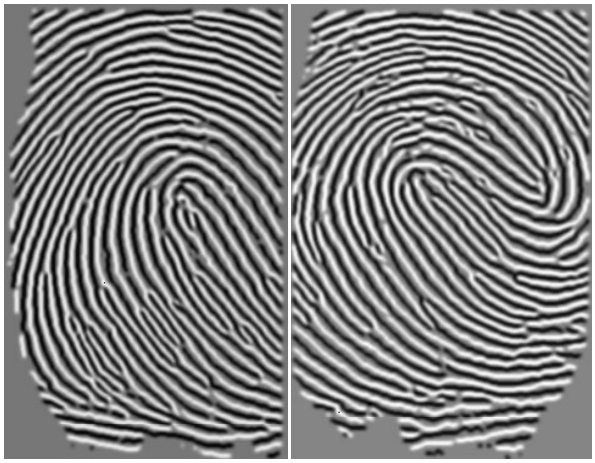

Figure 12.2.7: Binarized fingerprint images.

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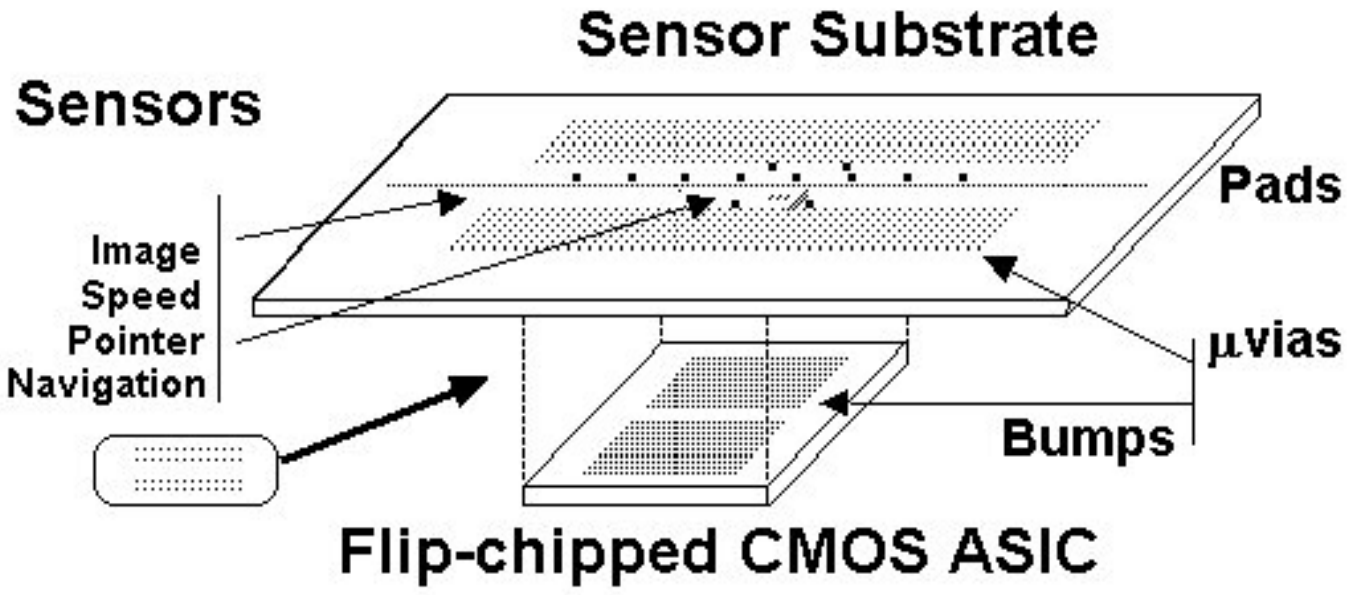

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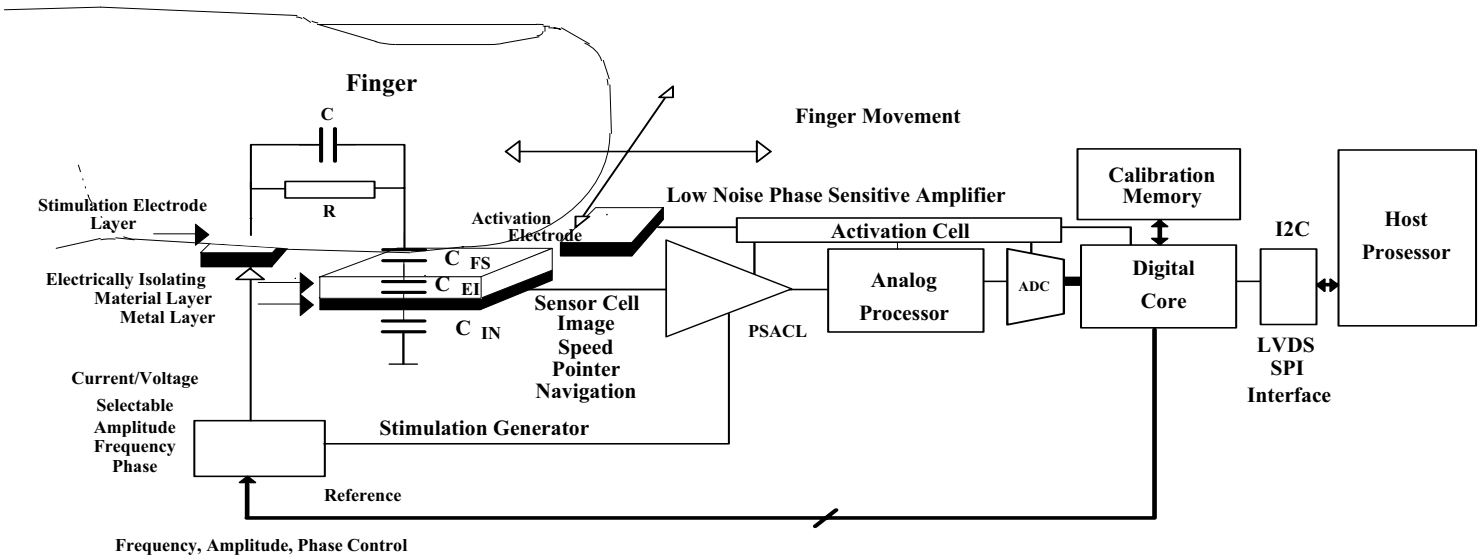


Figure 12.2.2: Module architecture.

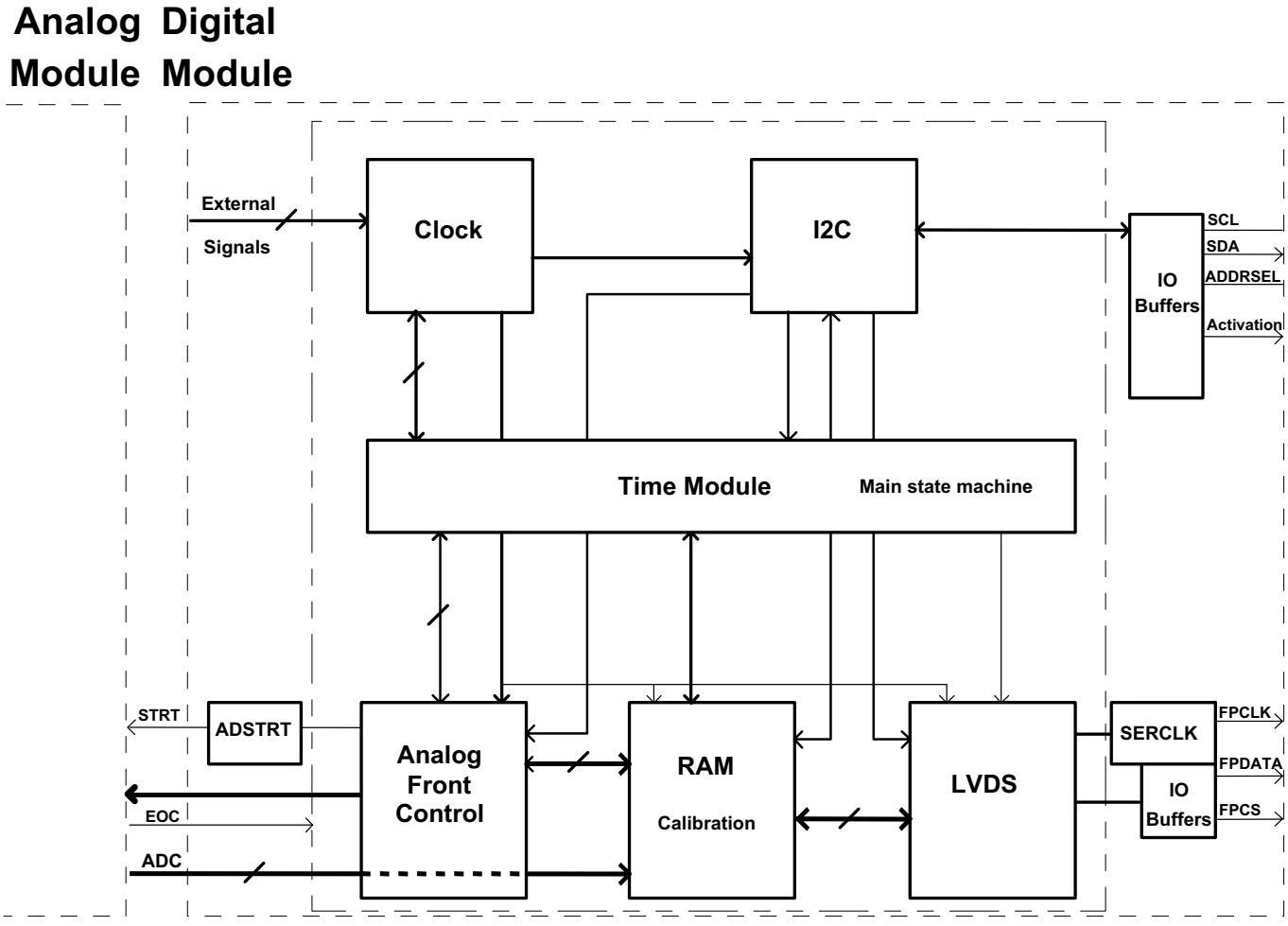
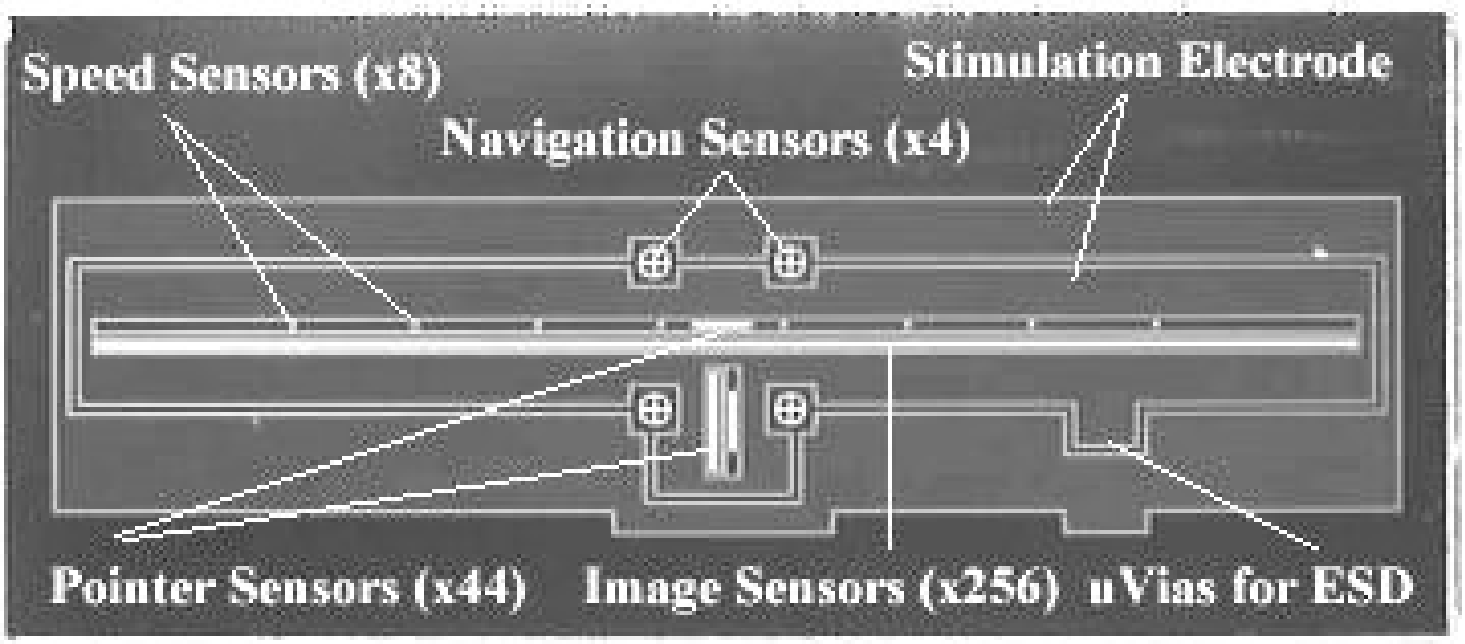


Figure 12.2.3: Digital core architecture.



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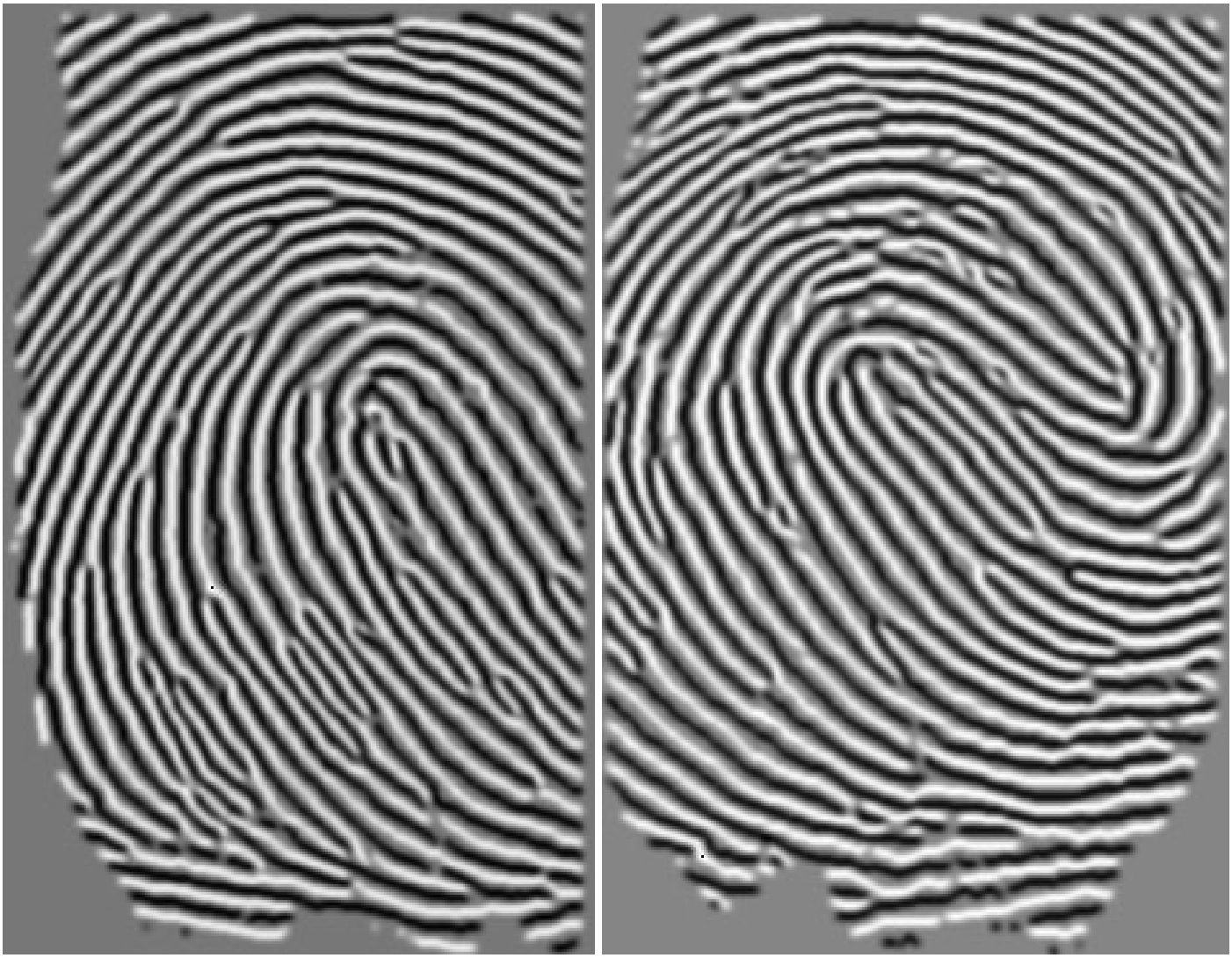

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